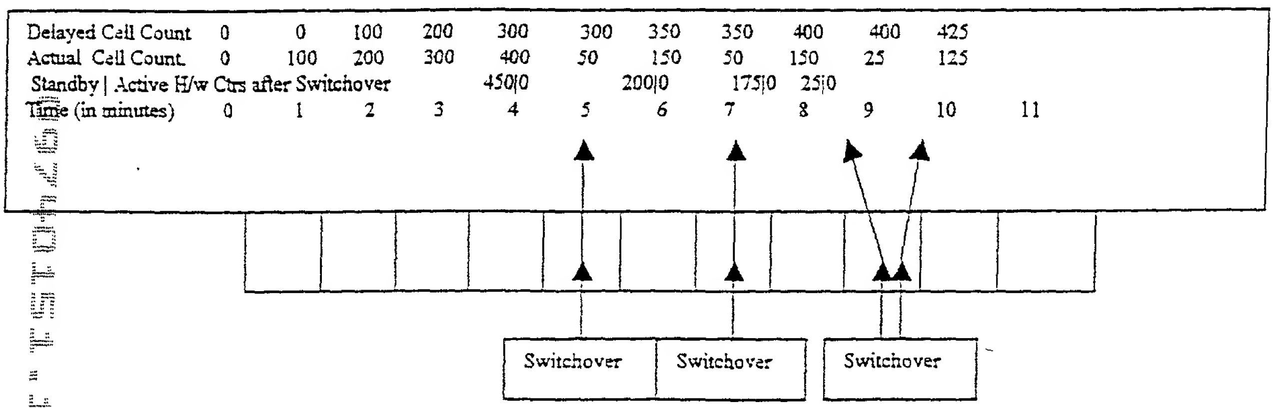
Delayed Cell Count 0 0 100 200 300 300 350 350 400 400 425
Actual Cell Count 0 100 200 300 400 50 150 50 150 25 125
Standby | Active H/w Ctrs after Switchover 450|0 200|0 175|0 25|0
Time (in minutes) 0 1 2 3 4 5 6 7 8 9 10 11
Switchover
Switchover
Switchover

Figure 1

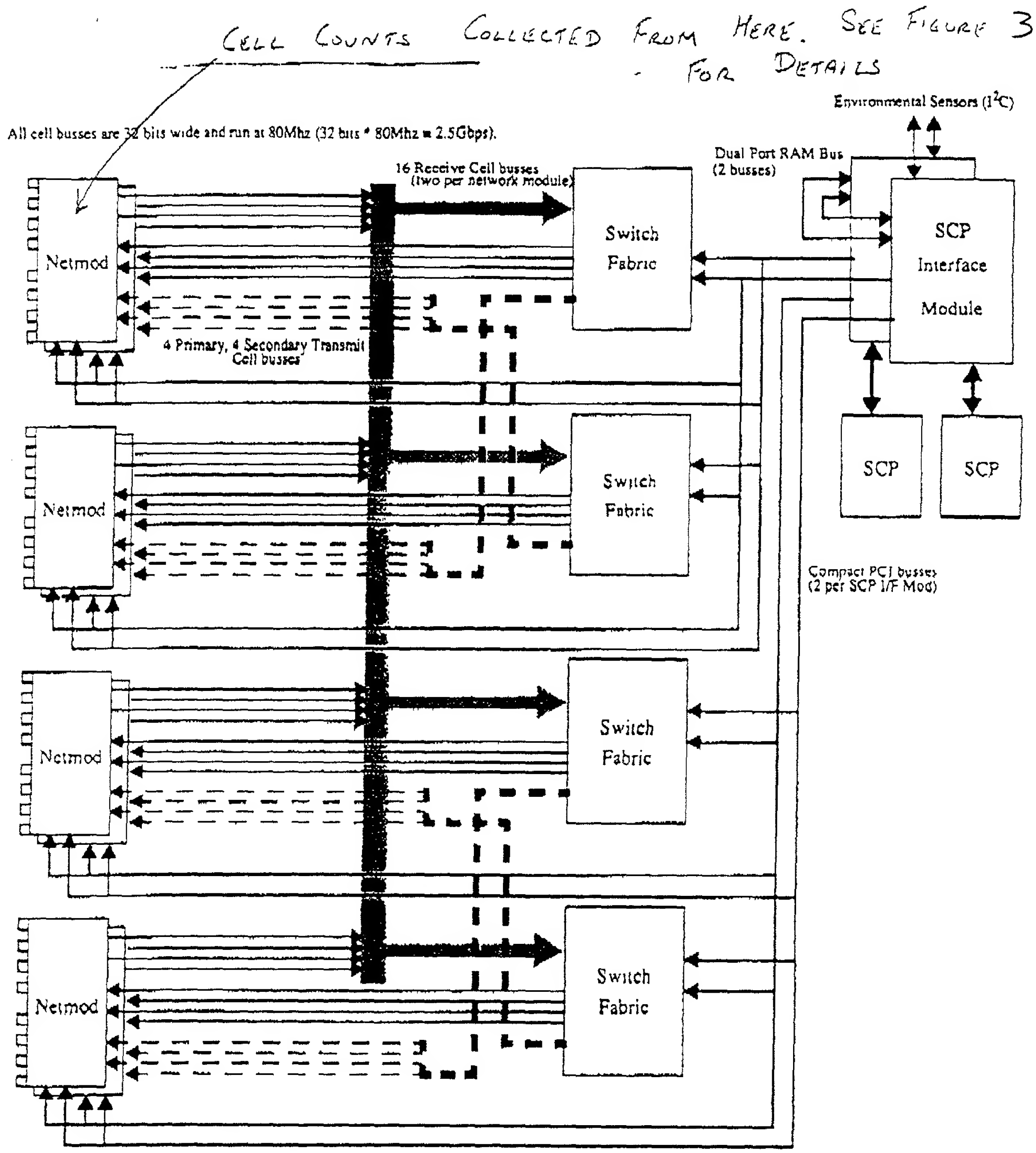
CELL COUNTS COLLECTED FROM HERE. SEE FIGURE 3 FOR DETAILS
All cell busses are 32 bits wide and run at 80Mhz (32 bits * 80Mhz = 2.5Gbps).
16 Receive Cell busses (two per network module)
4 Primary, 4 Secondary Transmit Cell busses
Netmod
Netmod
Netmod
Netmod
Switch Fabric
Switch Fabric
Switch Fabric
Switch Fabric
Environmental Sensors (I^2C)
Dual Port RAM Bus (2 busses)
SCP Interface Module
SCP
SCP
Compact PCI busses (2 per SCP I/F Mod)

FIG 2

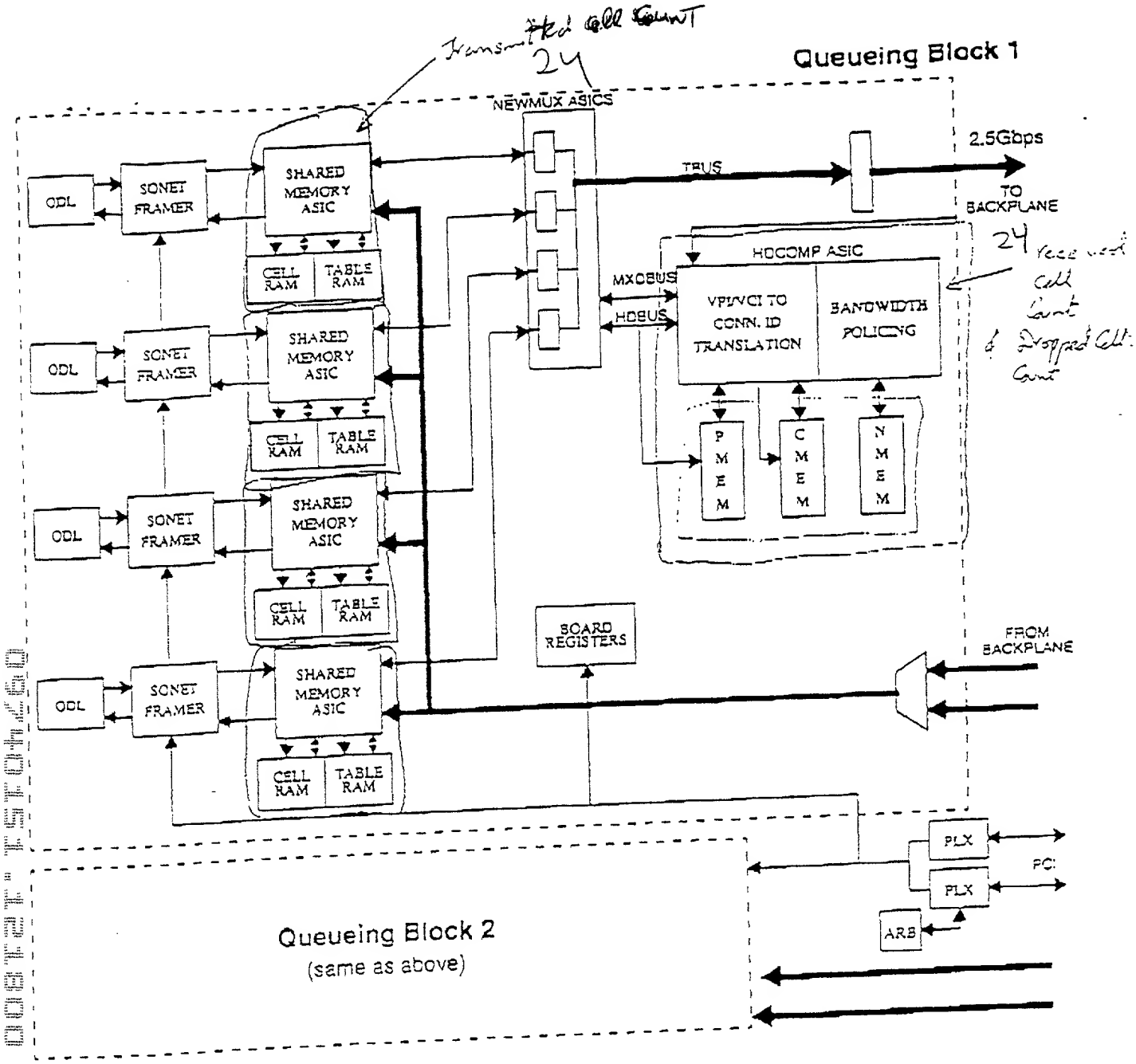
Queueing Block 1
NEWMUX ASICS
2.5Gbps
TO BACKPLANE
TRUS
ODL
SONET FRAMER
SHARED MEMORY ASIC
CELL RAM
TABLE RAM
MXDBUS
HDBUS
HDCOMP ASIC
VPI/VCI TO CONN. ID TRANSLATION
BANDWIDTH POLICING
PMEM
CMEM
NMEM
BOARD REGISTERS
FROM BACKPLANE
PLX
PCI
ARB
Queueing Block 2
(same as above)

FIG. 3

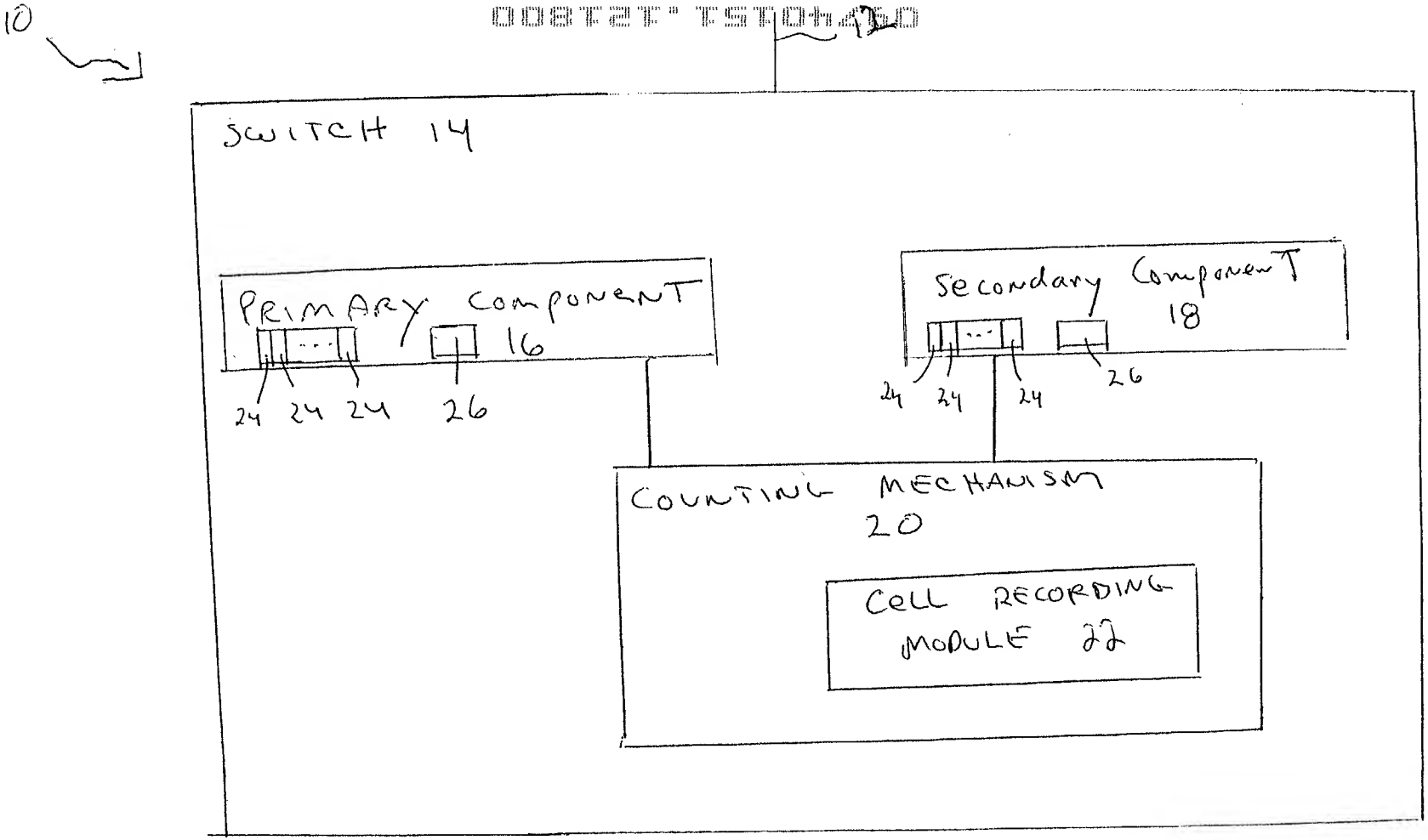
10
SWITCH 14
PRIMARY COMPONENT
16
24
24
24
26
Secondary Component
18
24
24
24
26
COUNTING MECHANISM
20
CELL RECORDING
MODULE 22

FIG 4